**Elevator Pitch**

**Motivation**

* Network-on-Chips (NoC) consume substantial amount of power of total chip power (about 10% – 36%)

**Proposal**

* Two approaches
  + Power-gating (PG) effective technique to reduce static power
  + Dynamic voltage and frequency scaling (DVFS) reduce dynamic power
* A combined approach of PG and DVFS is idea but overemphasizing one over the other causes problems
* Proposal
  + PG and DVFS combines design where PG disconnects from power supply when router is idle
  + RL-based control policy for combine design
  + ANN to reduce overhead cost of RL on per-router basis

**Experiments**

* Baseline: some NoC router with some sort of PG and DVFS logic, PID design
* Proposed design has 30% dynamic power savings
* Proposed design improved upon PID design by 13%
* Proposed design improved static power consumption by 16%
* Proposed solution has average 26% power reduction
* ANN reduces memory cost significantly yet can still achieve good accuracy